REMARKS

Present Status of Patent Application

Claims 1-16, and 18-20 remain pending of which claims 1, 9, 14, and 21 has been amended to more explicitly and more clearly describe the claimed invention. It is believed that no new matter adds by way of these amendments made to the claims or specification, or otherwise to the application. For at least for the following reasons, Applicant respectfully submits that claims 1-16, and 18-21 patently define over the prior art of record. Reconsideration is respectfully requested.

Response to Claims Rejections under 35 USC§103

1. The Office Action rejected claims 1-16, and 18-21 under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi et al. (US-6,118,154, hereinafter Yamaguchi) in view of Hu et al. (US-6,121,077, hereinafter Hu), Erdeljac et al. (US-5,554,873, hereinafter Erdeljac) and Japanese Patent #4-76959 (hereinafter JP).

In rejecting the above claims, the Office Action stated that the diode of figure 22 of Yamaguchi et al. is not related to the MOS diode 34 of the figure 19, but rather to diode 39 of figure 17 (see column 5, lines 3-5). Furthermore, a MOS diode would include source and drain regions. However, source and drain regions are not present in figure 22. Therefore, although Yamaguchi et al. categorize diode 39 as gate diode, it is not clear that diode 39 is a MOS diode. Please note that although MOS diode can be distinguished from non MOS diode, only claim 21 recites that limitation.

Applicants respectfully disagree and traverse the above rejections as set forth below. Independent claims 1, 9, 14, and 21 are allowable for at least the reason that Yamaguchi, Hu, Erdeljac, and JP failed to teach, suggest, or disclose every features of the claimed invention. More specifically, Yamaguchi, Hu, Erdeljac, and JP failed to teach, suggest or disclose an ESD protection circuit including at least ***"a single crystal sided junction diode without a control gate electrode, as required by claims 1, 9, 14, and 21".*** The advantage of including the above structure in an ESD protection circuit is that at least it allows a more simplified process for fabricating the above structure, thus the through-put can be substantially increased and also this would substantially reduce the manufacturing cost.

Instead, substantially, Yamaguchi in FIG. 22 shows a structure comprising gate control diode 38 and 39, wherein an anode region 38b, and cathode regions 38e and 38c form the gate control diode 38, and a cathode region 39c and anode regions 39b and 39e form the gate control diode 39. Therefore, clearly, FIG. 22 of Yamaguchi does not show a single crystal sided junction diode, instead shows a ppn gate control diodes 38 having a gate control gate 38a and another pnn gate control diode 39 with a control gate electrode 39a. Whereas, the claimed invention requires a single crystal sided junction diode without a gate electrode. Accordingly, Applicants respectfully submit that Yamaguchi cannot meet the claimed invention in this regard.

Further, substantially Yamaguchi teaches a gate oxide in between the gate electrode 38a/39a and the pnn/ppn doped regions. Since the claimed invention does not require a gate electrode, therefore there is no need of a gate oxide. In other words, therefore, in order to

fabricate the gate control diodes (38 and 39) of Yamaguchi, one needs to fabricate at least the ppn/pnn doped regions, the gate electrode 38a/39a and the gate oxide layer 38d/39d. Whereas, since the claimed invention substantially shows the use of a single crystal sided diode without a control gate electrode, and a gate oxide layer, and therefore the need for fabricating a control gate electrode and gate oxide can be effectively eliminated. Thus the through-put can be substantially increased and the cost of manufacture can be substantially reduced. Accordingly, Applicants respectfully submit that Yamaguchi cannot meet the claimed invention in this regard.

Further, since the Office Action relied upon Erdeljac and JP to disclose the silicon resistor, still Erdeljac and JP cannot cure the specific deficiencies of Yamaguchi. And similarly, since the Office Action relied upon Hu for disclosing an ESD protection circuit having an SOI structure formed on a mono-crystalline silicon, and therefore Hu cannot cure the specific deficiencies of Yamaguchi.

Applicants respectfully submit that since the remaining claims 1-8, 10-16, and 18-20, either depend directly or indirectly from the independent claims 1, 9, 14, therefore, they are also allowable over the prior art for at least the reasons as substantially discussed above.

For at least the foregoing reason, Applicant respectfully submits claims 1-16, and 18-21 patently define over prior art of record. Reconsideration and withdrawal of these rejections is respectfully requested.

CONCLUSION

For at least the foregoing reasons, it is believed that all pending claims 1-16, and 18-21 are in proper condition for allowance. If the Examiner believes that a conference would be of value in expediting the prosecution of this application, he is cordially invited to telephone the undersigned counsel to arrange for such a conference.

Respectfully submitted,
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Version with markings to show changes made

In the Claims:

Claims 1, 9, 14 and 21 have been amended as follows:

1. (Thrice Amended) An ESD protection structure having a single crystal Si-sided diode used to protect an internal circuit, the ESD protection structure electrically connected between an input pad and a node and the internal circuit electrically connected to the node, the ESD protection structure comprising:

a single crystal Si resistor formed over an insulating material layer, electrically coupled between the input pad and the node, wherein the single crystal Si resistor is horizontally isolated by an isolation structure; and

at least a single crystal silicon-sided junction diode without a control gate electrode formed over the insulating material layer, wherein the single crystal silicon-sided junction diode is electrically coupled between one terminal of a corresponding power supply and a node.

9. (Thrice Amended) An ESD protection structure having a single crystal Si-sided diode used to protect an internal circuit formed from an insulating material layer on a SOI, the ESD protection structure electrically connected between an input pad and a node and the internal circuit electrically connected to the node, the ESD protection structure comprising:

an input resistor including a plurality of single resistors formed over the insulating material layer, wherein each of the single resistors is electrically coupled between the input pad and the node, wherein the single crystal resistors is horizontally isolated by an isolation structure therebetween; and

at least a single crystal sided junction diode without a control gate electrode formed over the insulating material layer, wherein the single crystal sided junction diode is electrically coupled between one terminal of a corresponding power supply and a node.

14. (Twice Amended) A semiconductor structure of ESD protection, the ESD protection electrically connects between an input pad and an integrated circuit, the semiconductor structure comprising:

a semiconductor substrate;

an insulating layer, formed on the semiconductor substrate;

at least a single crystal Si resistor, formed over the insulating layer;

at least a single crystal Si-sided junction diode without a control gate electrode, formed over the insulating layer, wherein the single crystal Si-sided junction diode does not includes a MOS transistor serving as a diode;

a first conductive layer, formed over the insulating layer, used to electrically connect one terminal of the single crystal Si resistor and the input;

a second conductive layer, formed over the insulating layer, used to electrically connect another terminal of the single crystal Si resistor and the integrated circuit; and

a third conductive layer, formed over the insulating layer, used to connect the single crystal Si-sided junction diode and the integrated circuit.

21. (Thrice Amended) An ESD protection structure used to protect an internal circuit, the ESD protection structure electrically connected between an input pad and a node and the internal circuit electrically connected to the node, the ESD protection structure comprising:

a single crystal Si resistor formed on an insulating material layer, electrically coupled between the input pad and the node; and

a single crystal layer formed over the insulating material layer, wherein the single crystal layer comprises at least two doped regions with different dopant types to form a side junction diode without a control gate electrode, and the side junction is electrically coupled between one terminal of a corresponding power supply and a node, wherein the side junction diode is not a MOS device that serves as a diode.